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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,522	06/25/2001	Edward Colles Nevill	550-241	5749

23117 7590 01/06/2005

NIXON & VANDERHYE, PC
1100 N GLEBE ROAD
8TH FLOOR
ARLINGTON, VA 22201-4714

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,522	NEVILL ET AL.	
	Examin r	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on th cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/03/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22, 24, and 25 have been considered. Claims 1-17, 22, 24, and 25 have been amended as per Applicant's request. Claims 23 and 26-28 have been cancelled as per Applicant's request.

Claim Objections

2. Claim 8 is objected to because of the following informalities: Please correct claim 8, line 1 from "The apparatus Apparatus..." to read --The apparatus ~~Apparatus~~--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8, 10, 13, 15-19, 21-22, and 24-25 are rejected under 35 U.S.C. 102(b) as being taught by Blomgren, U.S. Patent Number 5,598,546 (herein referred to as '546) which incorporates Blomgren et al., U.S. Patent Number 5,781,750 (herein referred to as '750) by reference in column 1, lines 6-9 and column 4, lines 10-13.

5. Referring to claim 1, '546 and '750 have taught an apparatus for processing data, said apparatus comprising:

a. A processor core operable to execute operations as specified by instructions of a first instruction set, said processor core having an instruction pipeline into which instructions of said first instruction set and instructions of a second instruction set

that are to be executed are fetched from a memory and along which instructions progress ('546 column 2, lines 34-35 and '750 Abstract; column 3, lines 59-65; column 5, lines 3-10; and Figure 2, element 36); and

b. An instruction translator operable to translate instructions of a second instruction set into translator output signals corresponding to instructions of said first instruction set ('750 Abstract; column 4, lines 13-21; column 5, lines 24-31 and 49-55; and Figure 2, element 36);

c. Wherein said instruction translator is within said instruction pipeline and translates instructions of said second instruction set that have been fetched into said instruction pipeline from said memory ('750 Abstract; column 4, lines 13-21; column 5, lines 24-31 and 49-55; and Figure 2, element 36);

d. At least one instruction of said second instruction set specifies a multi-step operation that requires a plurality of operations that may be specified by instructions of said first instruction set in order to be performed by said processor core ('750 Abstract; column 4, lines 13-21; column 5, lines 24-31 and 49-55; and Figure 2, element 36); and

e. Said instruction translator is operable to generate a sequence of translator output signals to control said processor core to perform said multi-step operation ('750 Abstract; column 4, lines 13-21; column 5, lines 24-31 and 49-55; and Figure 2, element 36).

6. Referring to claim 2, '546 and '750 have taught wherein said translator output signals include signals forming an instruction of said first instruction set ('750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36).

7. Referring to claim 3, '546 and '750 have taught wherein said translator output signals include control signals that control operation of said processor core and are the same as control signals produced on decoding instructions of said first instruction set ('750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36).

8. Referring to claim 4, '546 and '750 have taught wherein said translator output signals include control signals that control operation of said processor core and specify parameters not specified by control signals produced on decoding instructions of said first instruction set ('750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36).

9. Referring to claim 5, '546 and '750 have taught wherein said processor core fetches instructions from an instruction address within said memory specified by a program counter value held by said processor core ('750 column 4, lines 47-49; column 6, lines 17-19; column 7, lines 37-40; and Figure 3).

10. Referring to claim 6, '546 and '750 have taught wherein, when an instruction of said second instruction set is executed, said program counter value is advanced by an amount that is independent of whether or not said instruction of said second instruction set specifies a multi-step operation ('750 column 4, lines 47-49; column 6, lines 17-19; column 7, lines 37-40; and Figure 3).

11. Referring to claim 7, '546 and '750 have taught wherein, when an instruction of said second instruction set is executed, said program counter value is advanced to specify a next

instruction of said second instruction set to be executed ('750 column 4, lines 47-49; column 6, lines 17-19; column 7, lines 37-40; and Figure 3).

12. Referring to claim 8, '546 and '750 have taught wherein said program counter value is saved if an interrupt occurs when executing instructions of said second instruction set and is used to restart execution of said instructions of said second instruction set after said interrupt ('750 column 5, lines 49-65; column 7, lines 33-35; and Figure 3). In regards to '750, it is inherent that the program counter value is saved when emulation mode is entered to process the interrupt in order for the CISC mode operation to resume with the next instruction, as stated in column 5, lines 63-65.

13. Referring to claim 10, '546 and '750 have taught wherein said processor has a register bank containing a plurality of registers and instructions of said first instruction set execute operations upon register operands held in said registers ('546 Abstract and '750 column 6, lines 60-63 and Figure 2).

14. Referring to claims 15 and 16, '546 and '750 have taught a computer program product including a computer program for controlling a computer to perform a method of processing data using a processor core having an instruction pipeline into which instructions of said first instruction set and instructions of a second instruction set that are to be executed are fetched from a memory and along which instructions progress, said processor core being operable to execute operations specified by instructions of a first instruction set ('546 column 2, lines 34-35 and '750 Abstract; column 3, lines 59-65; column 5, lines 3-10; and Figure 2, element 36), said method comprising the steps of:

a. Fetching instructions into said instruction pipeline ('750 column 6, lines 17-19); and

b. Translating fetched instructions of a second instruction set into translator output signals corresponding to instructions of said first instruction set using an instruction translator within said instruction pipeline ('750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36); wherein

c. At least one instruction of said second instruction set specifies a multi-step operation that requires a plurality of operations be specified by instructions of said first instruction set in order to be performed by said processor core ('750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36); and

d. Said instruction translator is operable to generate a sequence of translator output signals to control said processor core to perform said multi-step operation ('750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36).

15. Referring to claim 17, '546 and '750 have taught apparatus for processing data, said apparatus comprising:

a. A processor core operable to execute operations as specified by instructions of a first instruction set, said processor core having an instruction pipeline into which instructions of said first instruction set and instructions of a second instruction set that are to be executed are fetched from a memory and along which instructions progress ('546 column 2, lines 34-35 and '750 Abstract; column 3, lines 59-65; column 5, lines 3-10; and Figure 2, element 36); and

b. An instruction translator operable to translate instructions of a second instruction set into translator output signals corresponding to instructions of said first instruction set wherein said instructions of said second instruction set are variable length instructions ('750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36);

c. Said instruction translator is within said instruction pipeline and translates instructions of said second instruction set that have been fetched into a fetch stage of said instruction pipeline from said memory ('750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36); and

d. Said fetch stage of said instruction pipeline includes an instruction buffer holding at least a current instruction word and a next instruction word fetched from said memory such that if a variable length instruction of said second instruction set starts within said current instruction word and extends into said next instruction word, then said next instruction word is available within said pipeline for translation by said instruction translator without requiring a further fetch operation ('546 column 7, lines 12-15 and '750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36).

16. Referring to claim 18, '546 and '750 have taught wherein said instruction buffer is a swing buffer ('546 column 7, lines 12-15 and '750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36).

17. Referring to claim 19, '546 and '750 have taught wherein said fetch stage includes a plurality of multiplexers for selecting a variable length instruction from one or more of said

current instruction word and said next instruction word ('546 column 6, line 66 to column 7, line 10; column 7, lines 55-67; and Figure 3).

18. Referring to claims 13 and 21, '546 and '750 have taught a bypass path within said instruction pipeline such that said instruction translator may be bypassed when instructions of said second instruction set are not being processed ('750 column 3, line 59 to column 4, line 6; column 5, lines 3-46; and Figure 2).

19. Referring to claim 22, '546 and '750 have taught

a. At least one instruction of said second instruction set specifies a multi-step operation that requires a plurality of operations be specified by instructions of said first instruction set in order to be performed by said processor core ('750 Abstract; column 4, lines 13-21; column 5, lines 24-31 and 49-55; and Figure 2, element 36); and

b. Said instruction translator is operable to generate a sequence of translator output signals to control said processor core to perform said multi-step operation ('750 Abstract; column 4, lines 13-21; column 5, lines 24-31 and 49-55; and Figure 2, element 36).

20. Referring to claims 24 and 25, '546 and '750 have taught a computer program product including a computer program for controlling a computer to perform a method of processing data using a processor core operable to execute operations as specified by instructions of a first instruction set, said processor core having an instruction pipeline into which instructions of said first instruction set and instructions of a second instruction set that are to be executed are fetched from a memory and along which instructions progress ('546 column 2, lines 34-35 and '750

Abstract; column 3, lines 59-65; column 5, lines 3-10; and Figure 2, element 36), said method comprising the steps of:

a. Fetching instructions into said instruction pipeline ('750 column 6, lines 17-19); and

b. Translating fetched instructions of a second instruction set into translator output signals corresponding to instructions of said first instruction set using an instruction translator within said instruction pipeline, wherein said instructions of said second instruction set are variable length instructions ('750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36);

c. Said instruction translator is within said instruction pipeline and translates instructions of said second instruction set that have been fetched into a fetch stage of said instruction pipeline from said memory ('750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36); and

d. Said fetch stage of said instruction pipeline includes an instruction buffer holding at least a current instruction word and a next instruction word fetched from said memory such that if a variable length instruction of said second instruction set starts within said current instruction word and extends into said next instruction word, then said next instruction word is available within said pipeline for translation by said instruction translator without requiring a further fetch operation ('546 column 7, lines 12-15 and '750 Abstract; column 4, lines 13-21; column 5, lines 24-55; and Figure 2, element 36).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 9, 11-12, 14, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren, U.S. Patent Number 5,598,546 (herein referred to as '546), which incorporates Blomgren et al., U.S. Patent Number 5,781,750 (herein referred to as '750) by reference in column 1, lines 6-9 and column 4, lines 10-13, as applied to claims 1, 10, and 17 above, in view of Dickol et al., U.S. Patent Number 5,898,885 (herein referred to as Dickol). '546 and '750 have not explicitly taught

a. Wherein instructions of said second instruction set specify operations to be executed upon stack operands held in a stack (Applicant's claim 9).

b. Wherein a set of registers within said register bank holds stack operands from a top potion of said stack (Applicant's claim 11).

c. Wherein said instruction translator has a plurality of mapping states in which different registers within said set of registers hold respective stack operands from different positions within said stack, said instruction translator being operable to move between mapping states in dependence upon operations that add or remove stack operands held within said stack (Applicant's claim 12).

d. Wherein said instructions of said second instruction set are Java Virtual Machine bytecodes (Applicant's claims 14 and 20).

23. Dickol has taught

a. Wherein instructions of said second instruction set specify operations to be executed upon stack operands held in a stack (Applicant's claim 9) (Dickol, Col.4 lines 42-61).

b. Wherein a set of registers within said register bank holds stack operands from a top potion of said stack (Applicant's claim 11) (Dickol, Col.2 lines 59-67).

c. Wherein said instruction translator has a plurality of mapping states in which different registers within said set of registers hold respective stack operands from different positions within said stack, said instruction translator being operable to move between mapping states in dependence upon operations that add or remove stack operands held within said stack (Applicant's claim 12) (Dickol Col.6 lines 27-40 and Col.7 lines 5-16).

d. Wherein said instructions of said second instruction set are Java Virtual Machine bytecodes (Applicant's claims 14 and 20) (Dickol, Col.3 lines 49-57).

24. However, '546 and '750 has taught that the system is not limited to x86 CISC instructions and PowerPC RISC instructions and that various types of instruction formats may be used in the system ('750 column 5, lines 3-10). A person of ordinary skill in the art at the time the invention was made, and as taught in Dickol, would have recognized that translating Java Virtual Machine instructions into RISC-type native instructions (Dickol, Col.3 lines 49-57) eliminates redundant execution steps and native code execution performance is improved (Dickol, Col.2 lines 17-39). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate translating Java Virtual Machine

instructions, as taught by Dickol, in the device of '546 and '750 to improve processor performance.

Response to Arguments

25. Examiner withdraws the objection to the abstract in favor of the amended abstract.

26. Examiner withdraws claim objections from the Office Action dated 30 June 2004 in favor of the amended claims and arguments.

27. Examiner withdraws the 35 CFR § 112, second paragraph rejection in favor of the amended claims.

28. Applicant's arguments with respect to claims 1-22, 24, and 25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
21 December 2004

RICHARD L. ELLIS
PRIMARY EXAMINER